14. (Amended) The semiconductor die as recited in claim 11, wherein the perimeter [edge] surface has a ground surface.

15. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter [edges] side surfaces extending [disposed] between the first planar surface and the second planar surface; and

at least one perimeter [edge] surface having a treated surface, the entire at least one perimeter [edge] side surface having a substantially smooth surface;

a layer of scribe material forming the perimeter side surfaces, the layer of scribe material surrounding the circuitry; and

the first planar surface and the second planar surface of the semiconductor die have an overall rectangular shape.

16. (Amended) The semiconductor die as recited in claim 15, wherein [the] each entire [edge] side surface comprises a ground surface.

17. (Amended) The semiconductor die as recited in claim 15, wherein the entire [edge] side surface comprises a polished surface.

18. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter [edges] side surfaces extending [disposed] between the first planar surface and the second planar surface; and

at least one perimeter [edge] side surface having at least two offset planar [edges] surfaces, where the offset planar [edges] surfaces are substantially parallel to each other, where at least one of the two offset planar surfaces of at least one perimeter side surface are substantially flat and smooth.

20. (Amended) The semiconductor die as recited in claim 18, wherein each perimeter side surface [edge] has offset planar [edges] surfaces.

21. (Amended) The semiconductor die as recited in claim 18, wherein each offset planar surfaces [edge] is substantially smooth and flat.

22. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter [edges] side surfaces extending [disposed] between the first planar surface and the second planar surface;

a layer of scribe material forming the perimeter side surfaces, the layer of scribe material surrounding the circuitry; and

means for treating [providing] one or more of the perimeter [edge] side surfaces of the semiconductor die to provide one or more of the perimeter side surfaces with one or more substantially [flat] treated, and smooth surfaces.

23. (Amended) The semiconductor die as recited in claim 22, wherein the entire perimeter [edge] side surface is a substantially smooth surface.

24. (Amended) The semiconductor die as recited in claim 22, wherein the at least one perimeter [edge] side surface has offset planar [edges] surfaces, where the planar [edges] surfaces are each substantially smooth and are substantially parallel to each other.

25. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter [edges] side surfaces extending [disposed] between the first planar surface and the second planar surface;

each perimeter [edge] side surface having offset perimeter planar [edges] surfaces, where

the perimeter planar [edges] surfaces are substantially parallel to each other, and the perimeter planar [edges] surfaces are treated, substantially smooth surfaces;

a layer of scribe material forming the perimeter side surfaces, the layer of scribe material surrounding the circuitry; and

the semiconductor die has an overall rectangular footprint.

35. (Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter [edges] side surfaces extending [disposed] between the first planar surface and the second planar surface; and

at least one perimeter [edge] side surface having two or more offset planar perimeter surfaces [edges], at least one perimeter side surface having a treated, substantially smooth surface, where the planar [edges] perimeter surfaces are substantially transverse to the first planar surface and the second planar surface.

36. (Amended) The semiconductor die as recited in claim 35, wherein each planar [edge] perimeter surface has an entirely flat, smooth surface.

38. (Amended) The semiconductor die as recited in claim 35, wherein the planar [edges] perimeter surfaces have ground surfaces.

39. (Amended) The semiconductor die as recited in claim 35, wherein the planar [edges] perimeter surfaces have polished surfaces.

40. (Amended) The semiconductor die as recited in claim 35, wherein the planar [edges] perimeter surfaces are substantially parallel to one another.